AMENDMENTS TO CLAIMS

• Please amend pending claims 1-4, 6-12, 14-18, and 20-25 as indicated below. A complete listing of all claims and their status in the application is as follows:

1. (currently amended) A network interface for processing an incoming ~~messages~~message sent by a client device to a server, comprising:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming ~~messages~~message and to assemble the incoming ~~messages~~message from a serial to a parallel form; and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming ~~messages~~message from a serial to a parallel form, recognize a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message, parse the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header, and provide the parsed HTTP message ~~headers~~header to the server.

2. (currently amended) The network interface as claimed in claim 1 further including:

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message ~~headers~~header.

3. (currently amended) The network interface as claimed in claim 1 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the server the parsed HTTP message ~~headers~~header in a compact form.

4. (currently amended) The network interface as claimed in claim 1 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the server the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit.

5. (original) The network interface as claimed in claim 1 wherein:

the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof.

6. (currently amended) The network interface as claimed in claim 1 wherein:

the HTTP message ~~headers~~header include HTTP cookies.

7. (currently amended) A network interface for processing an incoming ~~messages~~message sent by a client device to a server, comprising:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming ~~messages~~message and to assemble the incoming ~~messages~~message from a serial to a parallel form;

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming ~~messages~~message from a serial to a parallel form, recognize a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message, parse the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header, provide the parsed HTTP message ~~headers~~header in a compact form to the server, and provide to the server the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit, wherein:

the HTTP message ~~headers~~header ~~include~~ includes a HTTP ~~cookies~~cookie, and

the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof; and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message header.

8. (currently amended) A server for providing services to a client device, comprising:

a central processing unit (CPU);

a bus connected to the CPU;

a memory connected to the bus, the memory having a server application program stored therein; and

a network interface for processing an incoming ~~messages~~message sent by the client device to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming ~~messages~~message and to assemble the incoming ~~messages~~message from a serial to a parallel form, and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming ~~messages~~message from a serial to a parallel form, recognize a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message, parse the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header, and provide the parsed HTTP message ~~headers~~header to the CPU and the memory, wherein the HTTP message ~~headers~~header ~~include~~includes a HTTP ~~cookies~~cookie.

9.   (currently amended)   The server as claimed in claim 8 further including:

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message ~~headers~~header.

10.   (currently amended)   The server as claimed in claim 8 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory the parsed HTTP message ~~headers~~header in a compact form.

11.   (currently amended)   The server as claimed in claim 8 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit.

12.   (currently amended)   The server as claimed in claim 8 wherein:

the HTTP message ~~headers~~header ~~include~~includes a HTTP ~~cookies~~cookie.

13.   (original)   A server for providing services to a client device, comprising:

a central processing unit (CPU);

a bus connected to the CPU;

a memory connected to the bus, the memory having a server application program stored therein; and

a network interface for processing incoming messages sent by the client device to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form,

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, provide the parsed HTTP message headers in a compact form to the CPU and the memory, and provide to the CPU and the memory incoming messages that cannot be recognized by the regular-expression pattern matching circuit, wherein: the HTTP message headers include HTTP cookies, and

the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof, and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers.

14.   (currently amended)   A communications network, comprising:

a client device; and

a server connected to the client device for providing services to the client device, the server including:

a central processing unit (CPU),

a bus connected to the CPU,

a memory connected to the bus, the memory having a server application program stored therein, and

a network interface for processing an incoming ~~messages~~message sent by the client device to the server, the network interface including:

a FIFO buffer adapted to receive the incoming ~~messages~~message and to assemble the incoming ~~messages~~message from a serial to a parallel form, and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming ~~messages~~message from a serial to a parallel form, recognize a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message, parse the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header, and provide the parsed HTTP message ~~headers~~header to the CPU and the memory.

15.   (currently amended) The communications network as claimed in claim 14 further including:

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message ~~headers~~header.

16.   (currently amended) The communications network as claimed in claim 14 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory the parsed HTTP message ~~headers~~header in a compact form.

17.   (currently amended) The communications network as claimed in claim 14 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit.

18.   (currently amended)   The communications network as claimed in claim 14 wherein:

the HTTP message ~~headers~~header ~~include~~includes a HTTP ~~cookies~~cookie.

19.   (original)   A communications network comprising:

a client device; and

a server connected to the client device for providing services to the client device, the

server including:

a central processing unit (CPU),

a bus connected to the CPU,

a memory connected to the bus, the memory having a server application

program stored therein, and

a network interface for processing incoming messages sent by the client device

to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming

messages and to assemble the incoming messages from a serial

to a parallel form,

a regular-expression pattern matching circuit connected to the FIFO

buffer, the regular-expression pattern matching circuit adapted

to, concurrent with the assembly of the incoming messages

from a serial to a parallel form, recognize Hypertext Transfer

Protocol (HTTP) message headers embedded in the incoming

messages, parse recognized HTTP message headers into parsed

HTTP message headers, provide the parsed HTTP message

headers in a compact form to the CPU and the memory, and

provide to the CPU and the memory incoming messages that

cannot be recognized by the regular-expression pattern

matching circuit, wherein:

the HTTP message headers include HTTP cookies, and

the regular-expression pattern matching circuit is implemented

by a technique consisting of hardware, software, and a

combination thereof, and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers.

20.   (currently amended)   A method for processing an incoming ~~messages~~message sent by a client device to a server, comprising:

receiving the incoming ~~messages~~message using a First-In-First-Out (FIFO) buffer;

assembling the incoming ~~messages~~message from a serial to a parallel form using the FIFO buffer; and

concurrent with the assembling of the incoming ~~messages~~message from a serial to a parallel form:

recognizing a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message received by the FIFO buffer using a regular-expression pattern matching circuit,

parsing the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header using the regular-expression pattern matching circuit, and

providing the parsed HTTP message ~~headers~~header to the server.

21.   (currently amended)   The method as claimed in claim 20 further including:

providing a response message to the client device based on a content of the recognized HTTP message ~~headers~~header.

22.   (currently amended)   The method as claimed in claim 20 wherein:

the providing the parsed HTTP message ~~headers~~header to the server provides the parsed HTTP message ~~headers~~header in a compact form.

23.   (currently amended)   The method as claimed in claim 20 further including:

providing to the server the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit.

24.   (currently amended)   The method as claimed in claim 20 wherein:

the HTTP message ~~headers~~header ~~include~~includes a HTTP ~~cookies~~cookie.

25. (currently amended) A method for processing an incoming ~~messages~~message sent by a client device to a server, comprising:

receiving the incoming ~~messages~~message using a First-In-First-Out (FIFO) buffer;

assembling the incoming ~~messages~~message from a serial to a parallel form using the FIFO buffer;

concurrent with the assembling of the incoming ~~messages~~message from a serial to a parallel form,

recognizing a Hypertext Transfer Protocol (HTTP) message ~~headers~~header embedded in the incoming ~~messages~~message received by the FIFO buffer using a regular-expression pattern matching circuit,

parsing the recognized HTTP message ~~headers~~header into a parsed HTTP message ~~headers~~header using the regular-expression pattern matching circuit, and

providing the parsed HTTP message ~~headers~~header to the server in a compact form;

providing a response message to the client device based on a content of the recognized HTTP message ~~headers~~header; and

providing to the server the incoming ~~messages~~message that cannot be recognized by the regular-expression pattern matching circuit.